行政院原子能委員會

委託研究計畫研究報告

以精煉冶金級矽(UMG-Si)為基板開發磊晶矽太陽能電池

Development of epitaxial silicon solar cells with UMG-Si substrates

計畫編號：992001INER043

受委託機關(構)：中原大學電子工程研究所

計畫主持人：籃山明

核研所聯絡人員：蘇郁涵

聯絡電話：03-2654637

E-mail address：onlyway54@hotmail.com

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目　錄

中文摘要

有鑑於近年來，各國對於太陽能電池需求量增加，導致矽原料的不足，其成本居高不下。以至於太陽能電池模組業者無不朝向太陽能電池薄型化，來確保產量以及降低成本。在降低成本方面，研發在低成本矽基板上製程技術，開發冶晶級矽太陽能電池，將可大幅減少高品質矽原料之使用。而本研究計畫嘗試使用廉價的提純級冶金矽(upgraded metallurgical silicon 簡稱 UMG-Si) 基板來研製太陽能電池。不容諱言，廉價的 UMG-Si 中存在許多的有害金屬雜質，關於此，我們將先以磷擴散吸雜法來加以純化，並製作成太陽能電池其效率皆可達 10 %以上。接著在 UMG-Si 基板背面上以常壓式有機金屬物化學氣相沈積法（ AP-MOCVD ）沉積氧化鋁薄膜，藉由 PERL (passivatedemitter,rearlocally-diffused)技術效提高 UMG-Si 太陽能電池轉換效率。最終其太陽能電池轉換效率可達 13.57%。

Abstract

In recent years, the demand of solar cells increases in the world, which causes the deficiency of silicon feedstock and therefore makes the cost of silicon raw material remain high. Resultantly, to stabilize both the output and price of solar cells the industry of solar cells has changed its production direction to thin-film solar cells. To lower the cost of solar cells, a device fabrication process based on the upgraded metallurgical silicon solar cells. In this plan, low-cost upgraded metallurgical grade silicon (UMG-Si) wafers have been used as the substrates to manufacture solar cells. Prior to device fabrication process, harmful impurities contained in UMG-Si substrates have been removed by phosphorus diffusion gettering, the photovoltaic conversion efficiency can achieve over 10 % for UMG-Si solar cell. Then we deposit the aluminum oxide on the substrate backside by metal-organic chemical vapour deposition, the photovoltaic conversion efficiency enhanced by the passivated emitter, rearlocally-diffused technology. The result obtained a high conversion efficiency of 13.57 % for UMG-Si solar cell can be presented in the present study.

壹、計畫緣起與目的

目前矽太陽能電池的發展，所使用矽基材主要分為四種等級，如表 1-1 所示。其中電子級矽與太陽能級矽，是目前太陽能產業使用最頻繁的，但有成本較高的問題，為了解決這問題，國外亦有將冶金級矽經由高溫再結晶並純化為精練冶金級矽(upgraded metallurgical grade Si, UMG-Si)的矽基板，然後再利用液相磊晶(liquid phase epitaxy, LPE)或化學氣相沈積(chemical vapor deposition, CVD)等方法製作磊晶矽太陽能電池，其成本和矽原料的使用相對減少許多，且轉換效率亦可達 10%以上。

表 1-1 矽基材種類與價位

Silicon grade	Si 純度	價位
冶金級(Metallurgical Grade Silicon, MG)	90-99%	USD: 1-2.5/kg
精練冶金級(Upgrade Metallurgical Grade Silicon , UMG)	99.9%	USD: 3-4/kg
太陽能級矽(Solar Grade Silicon, SG)	99.99-99.999%	USD: 30-40/kg
電子級矽(Electronic	>99.9999%	USD: Over 60/kg

Grade Silicon, EG)		

最早提出以 UMG-Si 基板製作矽太陽能電池者，首推美國國家再生能源實驗室(25th PVSC, May 13-17, 1996, Washington, D.C)，該團隊以低價位 UMG-Si 做為基板，在其兩面以簡單的腐蝕方法形成孔隙狀矽(porous silicon 厚約 2μm)，再經 1000℃、15-30 分鐘的退火處理後，將孔隙狀矽層去除掉，然後在基板上磊晶生長一層磊晶層做為太陽能電池的吸收層，雖然沒有報告其太陽能電池的轉換效率，但該團隊採用二次離子質譜儀(SIMS)方法分析銅原子在基板內的分佈，發現退火處理後銅雜質會從基板的內部擴散至基板的表面，證明此法處理有外部去疵的現象。而比利時 IMEC 公司在正式學術期刊發表其成果[Prog. photovolt：Res. Appl. 2005；13：673-690]，該公司從 2002 以來，開始以 UMG-Si 作為基板，採用磷擴散去疵與矽磊晶技術，所開發的矽太陽能電池其轉換效率介於 12-13%之間；若在磊晶之前，先在基板上添加孔隙狀矽反射層(PS reflector)其轉換效率可達 13.5%，但該公司的終極目標為 15%，以達到商用水準。

至於國內在此方面的研究，僅知工研院有一團隊在研究開發 UMG-Si 材料，據了解目前可將 UMG-Si 的純度提煉至 5N，另外在核研所有一開發團隊以工研院的 UMG-Si 做為基板，致力於開發研

究矽磊晶太陽能電池，但在國內學術團體則尚未有這方面的研究。

本計畫之目的乃迎合政府環保能源之既定政策，擬開發一個研製低價位磊晶矽太陽能電池的技術。而將矽磊晶技術應用於研製太陽能電池而言，將具有可提供一高品質的太陽能電池主動層(active layer)，進而提升轉換效率、在磊晶層與基板之間的界面可提供一反射層，增加光吸收量，進而提升轉換效率及可節省矽原料使用量，並取代目前塊材矽太陽能電池等幾項優勢：

因此，本計畫將使用 UMG p-Si 基板，藉由常壓式鹵化物化學氣相沈積法(atmospheric pressure halide chemical vapor deposition, APHCVD)，製作高品質的 p 型矽磊晶層，來當作太陽能電池的主動層(base layer)，其厚度與基板共約為 25-30 μm，此厚度範圍小於電子擴散長度，如此一來電子在擴散的過程中，不會因為主動層太厚，在還沒被電極收集以前就被複合；同時也大幅減少了矽原料使用量。而在製作 p 型矽磊晶層之前，由於 UMG-Si 基板本身存在許多缺陷及有害雜質(例如：鐵、銅和鎳等雜質)，因此，我們採用磷擴散吸雜法(Phosphorus Diffusion Gettering，PDG) 來做外部去疵，接著我們亦將利用背部表面電場(back surface field, BSF) 層結構及射極鈍化背面局部擴散來增加太陽能電池轉換效率，對於入射陽光所產生的少數載子可提供有效的驅回作用，減少表面複合，提高短路電流，我們預期最終將可達成研製轉換效率達 13%以上之低價位磊晶矽太陽能電池之目標。

貳、研究方法與過程

為了降低所使用矽材料的成本，本計畫使用相對廉價的UMG-Si基板來研製太陽能電池，標準製程如圖 2.1 所示，除導入外部去疵的方法來降低基板內部有害金屬雜質，同時為了在轉換效率上亦能具競爭優勢，在太陽能電池的背表面層部分係採用由常壓式化學氣相沉積(AP-MOCVD)所製作氧化鋁薄膜層，最終形成所謂 PERL 精煉冶金級矽太陽能電池結構。

一、標準製程

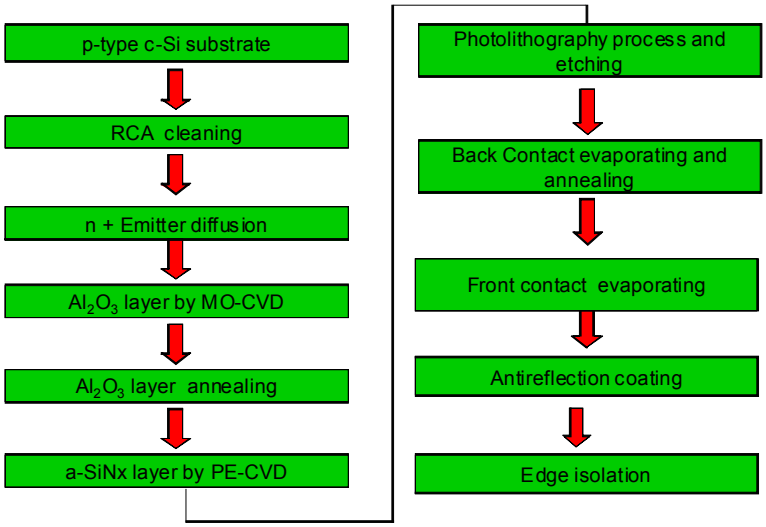


圖 2.1 太陽能電池的標準製程流程圖。

二、PERL 的製作

PERL 製作主要分為下列六個步驟：

(一)利用磷原子擴散製作 n^+-Si 射極層(emitter layer)

在 p-type UMG-Si 基板經過 RCA 標準清洗步驟，完成晶片清洗後，接著製作射極層使之與主動層形成之 pn 接面，來提供內建電場，並未有吸收光能之功用，所以在製作時以厚度薄為主要目標，避免光在尚未到達 pn 接面時，

就被射極層所吸收。

(二)以 AP－MOCVD 法製作介電材料 Al_2O_3

在本實驗中，採用 alternating trimethylaluminium(TMA)與氧氣(O_2)做為沉積 Al_2O_3 介電層的來源，承載氣體為氮氣。成長溫度：350~450℃，時間：10-20 分鐘。

完成 p 型區域成長介電層後，將利用電容電壓(C-V)量測系統(Agilent B1500A)確認其帶負電荷，預期帶電荷約為 10^{10}~10^{12} cm^{-2}，於此範圍有最大的轉換效率(資料來源：B. Hoex, S. B. S. Heil, E. Langereis, et.al, Applied Physics Letters 89, 042112 (2006)。而一般於太陽能電池的結構上，pn 接面照光後會產生少數載子電子、電洞流，由於內建電場的驅使下，會使電子往 n 型區域擴散，而電洞往 p 型區域擴散，而 p 型區域上帶負電荷的氧化鋁，可以對入射陽光所產生的少數載子電洞提供有效的吸引作用，進而提高短路電流，增加轉換效率，此乃本計畫論文之重點。在圖 2.2 中，自由電洞的行進方向在界面處就會受到氧化鋁帶電荷的牽制。圖中左側區域主要收集自由電洞，自由電子則往右側擴散。

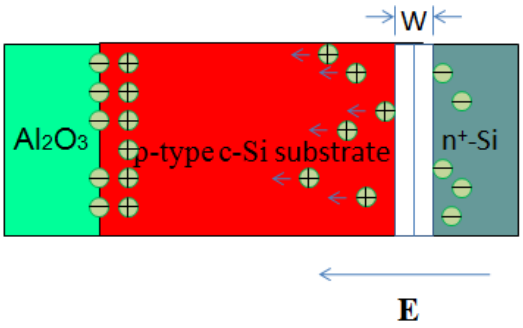


圖 2.2 自由電子與電洞行進方向示意圖

(三)以 PECVD 法製作介電材料 SiN_X

接著在氧化鋁薄膜上沉積可增加 rear light collection 之材

料，本計畫將選用氮化矽(SiN_x)，其折射係數 n=2，可利用電漿輔助化學氣相沉積(PECVD)系統成膜，其 Si 與 N 的氣體源分別使用 SiH_4 和 NH_3。

(四)微影蝕刻製作背電極接觸孔洞

本計畫背電極孔洞之製作是在介電層 a-SiNx 上以旋轉塗佈機佈上負阻，在軟、硬考之後，在使用設計之光罩(面積為 80nm x 80nm，孔洞間距 1000 μm，直徑為 100~200 μm)曝光，而後顯影，再以稀釋氫氟酸($HF:H_2O=1:10$)蝕刻介電層(a-SiNx、Al_2O_3)形成接觸孔洞。

(五)正背面電及製作及正面抗反射層

正電極必須形成歐姆接觸，提供外部電路與太陽能電池之間相互傳導的一個低電阻接面，另外還有接收載子的功用。選擇正電極材料時須考量其是否能形成良好的低阻值歐姆接觸?以及是否會影響光的吸收？所以本研究所研製之磊晶矽太陽能電池將使用 Ti/Pd/Ag 金屬當正電極。

背電極的功用如同正電極，但是因為不用考慮到是否影響光吸收的問題，所以可選擇導電性良好的金屬，直接將金屬以電子束蒸鍍機鍍在基板上形成一層金屬膜(Al)，再藉由回火，使其與基板形成歐姆接觸。

在元件上增加表面粗糙化及抗反射層的製作，可以有效減少光反射率，而本實驗抗反射層採用氮化矽(a-SiNx)，在經由實驗之後，可得到其對光反射率可有效降低 30~35%，其對各波長抗反射效果如下圖 2.3 所示。

完成上述的步驟後，可得一 PERL 型 UMG-Si 太陽能電池結構，其結構如下圖 2.4 所示。

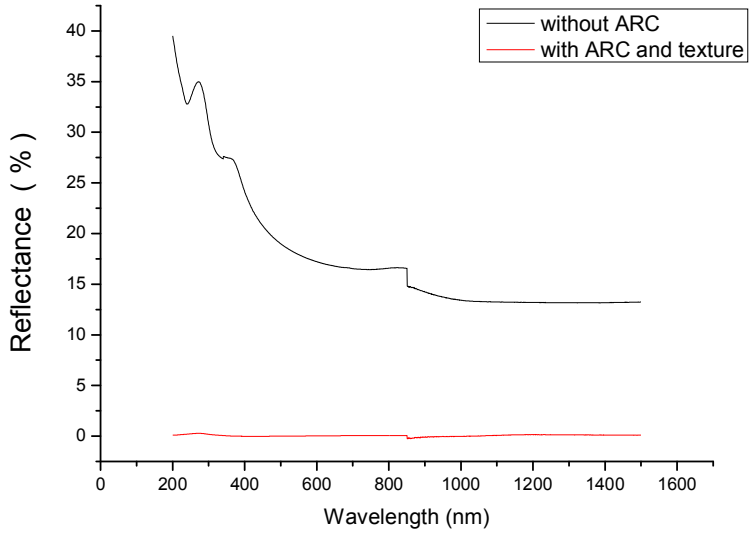


圖 2.3 加入表面粗化及 SiNx 抗反射層前後的反射率比較圖

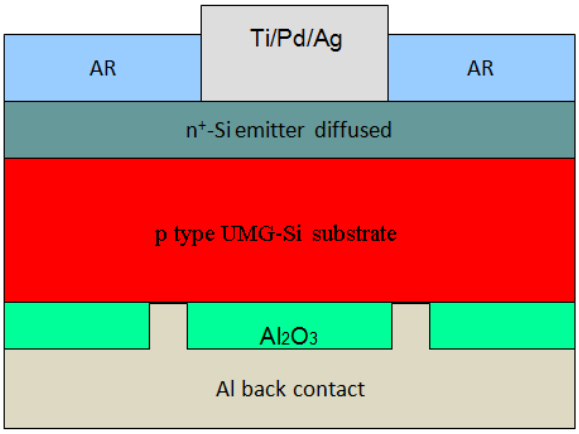


圖 2.4 PERL 型 UMG-Si 太陽能電池示意圖

參、主要發現與結論

實驗結果首先印證氧化鋁薄膜層是否帶負電荷，其結果如下表一所示，氧化鋁薄膜層在525℃的成長條件下，所帶的電荷量為Q_{SS}=-8.75x$10^{11}$$cm^{-2}$，此與文獻中內建負電荷(Qf= 10^{10}~10^{12} cm^{-2})即可應用在太陽能電池的p型區域上，可加強少數載子電動流的收集的論點相府和。在確認氧化鋁薄膜層具有帶負電的效果之後，為進一步確認其有背表面頓化效果，我們嘗試在用450℃沉積完氧化鋁薄膜後，藉由不同的回火條件，分別少數量測其載子生命週期(lifetime)，以求其最佳的表面鈍化效果。其結果分別由下表二及表三所示，在量測其少數載子生命週期後，可得氧化鋁薄膜最佳的回火條件為500℃、30分鐘。

接著我們先用基本製程用磷擴散作n-p介面，再蒸鍍上正反電極做為太陽能電池元件當作基準片，其I-V量測太陽能轉換效率為10.44%；再利用前述的實驗方法將氧化鋁薄膜沉積於p型基板背面，其轉換效率最高為13.57%，分別記錄於下表四、表五。我們可以明顯的發現其轉換效率比未做PERL技術多了接近3%的。由此結果我們可以證實了氧化鋁薄膜沉積在p型基板背後確實有鈍化效果，並增加了少數載子的壽命，降低表面複合速率，所以太陽能轉換效率才有顯著提升。

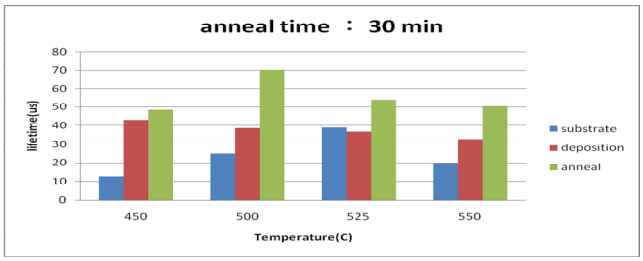
由上述結果可知利用PERL技術太陽能轉換效率可以有顯著的提升。我們再繼續氧化鋁薄膜作探討，我們利用常壓式有機金屬物化學氣相沈積法沉積氧化鋁薄膜，我們試著改變不同的沉積時間來探討不同的氧化鋁薄膜沉積厚度對於效率是否改變。

圖 3.1 為氧化鋁沉積不同時間的 SEM 圖，沉積時間分別為 10 分鐘、15 分鐘、20 分鐘，厚度分別為 100.6nm、165nm、185nm，其成長速率則分別為 10nm/m、11nm/m、9.2nm/m，此時我們可以發現隨著沉積的時間增加，其氧化鋁薄膜沉積速率也逐漸下降。此時我們再將沉積不同時間的氧化鋁薄膜作成太陽能電池元件並用 I-V

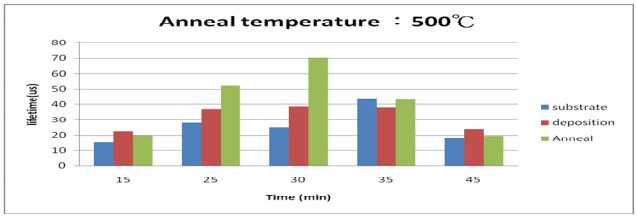
量測太陽能轉換效率，表二為量測結果。表二結果顯示，隨著氧化鋁薄膜度增加，太陽能轉換效率會逐漸下降，在此我們可以知道太陽能轉換效率是會被氧化鋁薄膜沉積的厚度所影響。

Sample	**T (℃)**	**TMA (umol/min)**	**O_2 (umol/min)**	**Q_{SS} (cm^{-2})**
Al_2O_3	525	14.3	1339	$-8.75x10^{11}$

表一 氧化鋁沉積條件及帶電量示意圖



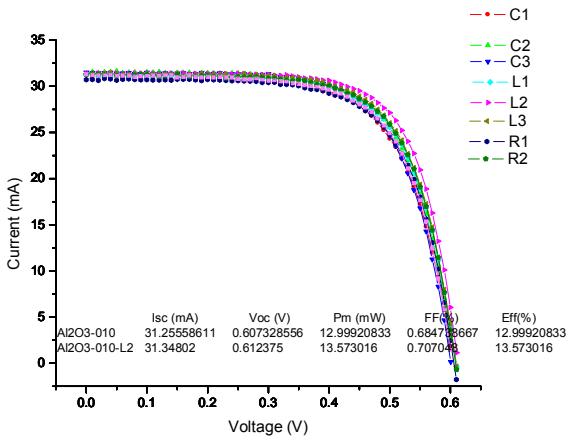
表二 分別針對 450℃、500℃、525℃、550℃條件做回火條件



表三 對 500℃做 15、20、25、30、35、45 分鐘回火

	Voc (V)	Isc(mA)	Pm(mW)	FF(%)	Eff(%)
未做 PERL	0.559377	29.14992	10.4419	0.64038	10.4419
PERL on UMG-Si	31.34802	0.612375	13.57302	0.707048	13.57302

表四 在 AM=1.5 下， I–V 量測太陽能電池轉換效率



表五 在 AM=1.5 下，PERL I–V 量測太陽能電池轉換效率

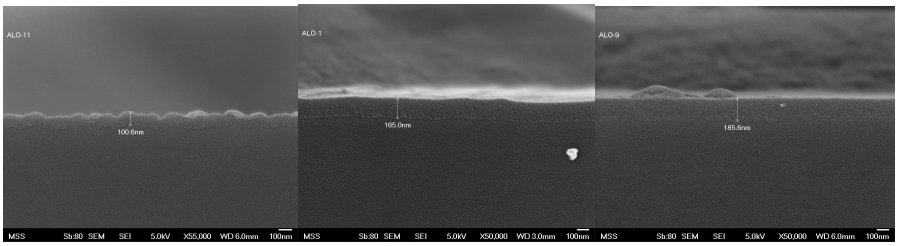


圖 3.1 由左至右分別為沉積氧化鋁薄膜 **10** 分鐘、**15** 分鐘、**20** 分鐘的 **SEM** 圖

結論

原子層沉積法（Atomic Layer Deposition, ALD）是現今沉積氧化鋁薄膜較常見的方式，但因為此方法較昂貴且生產量小，所以我們利用常壓式有機金屬物化學氣相沈積法（AP-MOCVD）沉積氧化鋁可以有效降低生產成本，在本研究裡氧化鋁薄膜成長最佳條件為450℃、10分鐘，回火溫度500℃、20分鐘，再利用PERL(passivated emitter, rear locally-diffused)技術可以有效提冶金級矽太陽能轉換效率，此技術有背面鈍化效果，並可以增加少數載子壽命。我們將未經過PERL技術處理的太陽能電池元件與有使用PERL技術的太陽能電池元件比較，有使用PERL技術其太陽能轉換效率可達13.57%，明顯提升近3%的效率。

此外，我們發現氧化鋁薄膜沉積時間不同也會改變其太陽能轉換效率，隨著氧化鋁沉積時間增加，太陽能轉換效率也會逐漸下降。

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伍、附註

國外期刊論文

1. Yen-Chin Huang, Li-Wei Weng, Wu-Yih Uen , Shan-Ming Lan, Zhen-Yu Li, Sen-Mao Liao, Tai-Yuan Lin, Tsun-Neng Yang, “Annealing effects on the p-type ZnO films fabricated on GaAs substrate by atmospheric pressure metal organic chemical vapor deposition”Journal of Alloys and Compounds xxx (2010) xxx–xxx
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國內研討會發表

1. Sz-Tseng Wu, Heng-Wei Lin , Shan-Ming Lan, Wu-Yih Uen, Tsun-Neng Yang, Jian-Wun Chen, Yu-Han Su, Yu-Hsiang Huang, Jin-jhan Jheng , Chin-Chen Chiang,“Improving the efficiency of multicrystalline silicon solar cells by using phosphorus diffusion gettering”, 2010 中國材料科學學會年會 04-0650, Taiwan.

2. Li-Wei Zeng , Heng-Wei Lin , Shan-Ming Lan, Wu-Yih Uen, Tsun-Neng Yang, Jian-Wun Chen, Yu-Han Su, Yu-Hsiang Huang, Jin-jhan Jheng , Chin-Chen Chiang,“研製高效率PERL(passivated emitter, rear locally-diffused)單晶矽太陽能電池”, 2010中國材料科學學會年會04-0975, Taiwan.

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Annealing effects on the p-type ZnO films fabricated on GaAs substrate by atmospheric pressure metal organic chemical vapor deposition

Yen-Chin Huang[a], Li-Wei Weng[a], Wu-Yih Uen[a,*], Shan-Ming Lan[a], Zhen-Yu Li[b], Sen-Mao Liao[a], Tai-Yuan Lin[c], Tsun-Neng Yang[d]

[a] Department of Electronic Engineering, College of Electrical Engineering and Computer Science, Chung Yuan Christian University, Chung-Li 32023, Taiwan
[b] Department of Photonics & Institute of Electro-Optical Engineering, National Chiao Tung University, 1001 TA Hsueh Road, Hsinchu 30010, Taiwan
[c] Institute of Optoelectronic Sciences, National Taiwan Ocean University, Keelung 222, Taiwan
[d] Institute of Nuclear Energy Research, P.O. Box 3-11, Lungtan 32500, Taiwan

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ABSTRACT

The effects of post-annealing conducted at 500–650 °C on structural, electrical and optical properties of ZnO film fabricated on GaAs (1 0 0) substrate by atmospheric pressure metal-organic chemical vapor deposition are investigated. X-ray diffraction analyses show that the Zn_3As_2 and $ZnGa_2O_4$ phases are produced for the specimens post-annealed at 500 °C and above. Hall measurements indicate that stable p-type ZnO films with hole concentration ranging from 4.7×10^{18} to 8.7×10^{19} cm^{-3} can be obtained by modulating the annealing temperature from 500 to 600 °C. In particular, room-temperature photoluminescence (PL) measurements indicate that the superior-quality p-type film could be achieved by a post-annealing treatment at 600 °C. Moreover, low temperature PL spectra at 10 K are dominated by the acceptor-related luminescence mechanisms for the films post-annealed at 550 °C and above. The ionization energy of acceptor was calculated to be 133–146 meV, which is in good agreement with that theoretically predicted for the $As_{Zn}–2V_{Zn}$ complex in ZnO. The interdiffused arsenic atoms in the film post-annealed at 600 °C are suggested to form the $As_{Zn}–2V_{Zn}$ complex quite effectively, resulting in the most enhanced p-type conductivity and improved material quality.

1. Introduction

Zinc oxide (ZnO) is a wide band gap semiconductor with a direct band gap of 3.37 eV at room temperature and a large exciton bind energy of 60 meV, which makes it a good candidate for the applications in highly efficient and stable room temperature ultra-violet (UV) lasers and light emitting diodes [1–3]. To achieve such goals, the growth of high-quality p-type ZnO is required. However, the fabrication of p-type ZnO films by doping is difficult due to the compensation effect of native n-type carriers released by the donor-type defects such as oxygen vacancies and zinc interstitials [4,5].

Recently, several groups have reported the growth of p-type ZnO by doping group V elements N [6], P [7], As [8], and Sb [9]; however, their behavior in the lattice and the corresponding electronic levels are poorly understood. Among the group V elements examined, nitrogen has been regarded as the most suitable impurity for p-type doping in ZnO due to its atomic radius is similar to that of oxygen. However, numerous experimental efforts made by different groups to implement this idea have not resulted in stable and reproducible p-type material yet. Moreover, J.L. Lyons et al. even reported that N is actually a deep acceptor in ZnO with an exceedingly high ionization energy of 1.3 eV based on their theoretical calculations [10]. Therefore, the suitability of N-doping for p-type conductivity in ZnO is required to be examined in more detail.

On the other hand, it seems convincing that the behavior of other group V elements, such as As and Sb, as acceptors in ZnO does not stem from a simple substitution on the group VI-site, but rather from complexes of the type $As(Sb)_{Zn}–2V_{Zn}$ with low enthalpies of formation [11]. A direct evidence for arsenic as a zinc-site impurity in ZnO has been presented by U. Wahl et al. using the emission channeling technique [12]. To achieve this purpose, several researchers have prepared ZnO films on GaAs substrates and annealed the specimens to have As atoms diffuse from the substrate into the ZnO films. In this way, p-type ZnO films have been obtained somehow under a strict annealing condition [6,13–15].

This work reports the p-type conductive behavior of ZnO films fabricated on semi-insulating GaAs substrate, regardlessly as-grown or post-annealed, using atmospheric pressure metal organic chemical vapor deposition (AP-MOCVD) technique. In particular, the effects of post-annealing on the p-type characteristics are systematically investigated by analyzing the structural, electrical, and

* Corresponding author. Tel.: +886 3 265 4620; fax: +886 3 265 4699.
E-mail addresses: chin099983@hotmail.com (Y.-C. Huang), uenwuyih@ms37.hinet.net (W.-Y. Uen).

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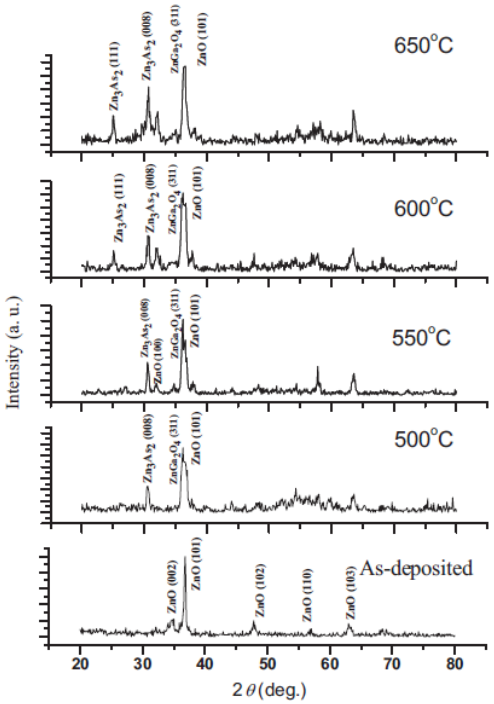

Fig. 1. XRD patterns of ZnO films as deposited and post-annealed at different temperatures from 500 to 650 °C.

optical properties of the films post-annealed at various temperatures. Additionally, the mechanisms responsible for the results obtained are discussed.

2. Experiment

ZnO thin films were deposited on the semi-insulating GaAs (1 0 0) substrate (henceforth, refer to as ZnO/GaAs) by a custom-made one-flow AP-MOCVD system. The growth chamber is a water-cooled vertical reactor. The substrate susceptor is made of graphite, 2 in. in diameter and coated with a SiC film on top surface by CVD technique. Diethylzinc (DEZn) and deionized water (H_2O) were used as the sources of Zn and O, respectively. The growth of ZnO layer was conducted at 450 °C with the flow rates of DEZn and H_2O maintained at 13.4 and 45.7 μmol/min, respectively to have a constant gas flow ratio of [H_2O]/[DEZn] (VI/II ratio) = 3.42. After growth, the 2-in.-diameter wafer was cut into small pieces with the size of 10 mm × 10 mm. Some of the specimens were further annealed in oxygen atmosphere using a rapid thermal annealing system to activate the p-type conductivity of films deposited. The temperature set for post-annealing treatment has been varied from 500 to 650 °C with an increase step of 50 °C. The crystal structure of ZnO thin films was analyzed by x-ray diffraction (XRD, Bruker AXS Diffraktometer D8) using Cu K_α line as the x-ray source (λ = 1.54056 Å) for a 2θ range 20–80°. The resistivity, carrier concentration and mobility of films were measured at room temperature by Hall measurements using the van der Pauw method. The optical properties were examined by photoluminescence (PL) measurements performed at room temperature and 10 K. PL spectra were excited by the 325-nm line of a He-Cd laser with an excitation power of 15 mW.

3. Results and discussion

The XRD patterns of the as-grown ZnO/GaAs(1 0 0) sample and those post-annealed at various temperatures ranging from 500 to 650 °C are shown in Fig. 1. Obviously, all the films show polycrystalline structure with various crystallographic planes being

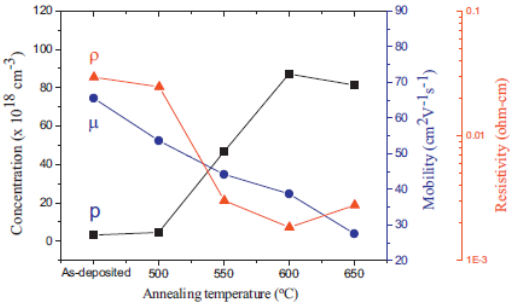

Fig. 2. Resistivity (ρ), mobility (μ), and carrier concentration (p) of ZnO films: as-deposited and post-annealed at different temperatures.

detected. The as-grown film exhibits a grain structure with a dominant plane orientation of (1 0 1). For the samples with the post-annealing conducted at 500 and 550 °C, the intensity of (1 0 1) peak greatly decreases and the XRD patterns become dominated by the other two diffraction peaks at about 30.4° and 35.8° instead. With a further increase in annealing temperature to over 550 °C, another diffraction peak appears at about 25.2°. The presence of XRD peaks at 25.2°, 30.4° and 35.8° demonstrate the formation of Zn_3As_2(1 1 1) [16], Zn_3As_2(0 0 8), and $ZnGa_2O_4$(3 1 1) [17] phases, respectively. These structures were formed due to the interdiffusion of As and Ga atoms into the deposited film, followed by the bonding reactions between them and host Zn and O atoms. The phases of Zn_3As_2 and $ZnGa_2O_4$ mentioned above were not found in previous reports concerned with the thermal diffusion effect on similar ZnO/GaAs material structures fabricated by various methods [6,13–15]. It is also noticeable that the intensities of Zn_3As_2(1 1 1), Zn_3As_2(0 0 8) and $ZnGa_2O_4$(3 1 1) increase with increasing annealing temperature. This manifests that the number of As and Ga atoms introduced into the AP-MOCVD grown film can be controlled by the annealing temperature.

Fig. 2 displays the resistivity (ρ), Hall mobility (μ) and hole concentration (p) of ZnO films as a function of the film annealing temperature. It is noteworthy that even the as-deposited ZnO has already shown p-type conductivity, with ρ, μ, and p measured as 2.954×10^{-2} Ω cm, 65.6 $cm^2 V^{-1} s^{-1}$, and 3.22×10^{18} cm^{-3}, respectively. As known, the intrinsic conductivity of ZnO is greatly influenced by the point defects produced therein. The p-type conductivity of undoped ZnO has been reported to be possibly due to the formation of Zn vacancies [18]. Our previous investigation also demonstrated that intrinsic p-type ZnO films with the hole concentration 1.5–3.3 × 10^{17} cm^{-3} can be achieved on Si(1 0 0) substrate [19]. In that study, we used the same precursors as now and also conducted the film growth in an oxygen-rich condition (VI/II ratio = 1.1–2.74) to have native defect V_{Zn} related acceptors be the origin of p-type conductivity. However, the elevation of about one order of magnitude in the hole concentration (3.22×10^{18} cm^{-3}) for the as-grown film here seems hard to be completely attributed to the same reasoning. As introduced before, arsenic should also play a part in the p-type doping, which would increase the free hole concentration in this film. Particularly, this behavior is emphasized by the post-annealing as described below. It can be seen that the resistivity of the deposited film decreases initially with increasing annealing temperature and reaches a minimum value of 1.85×10^{-3} Ω cm at the annealing temperature = 600 °C. Then it increases conversely with a further increase of annealing temperature to 650 °C. Whereas, the hole concentration increases gradually with increasing the annealing temperature from 500 to 600 °C and reaches a maximum value of 8.72×10^{19} cm^{-3}. However, a further

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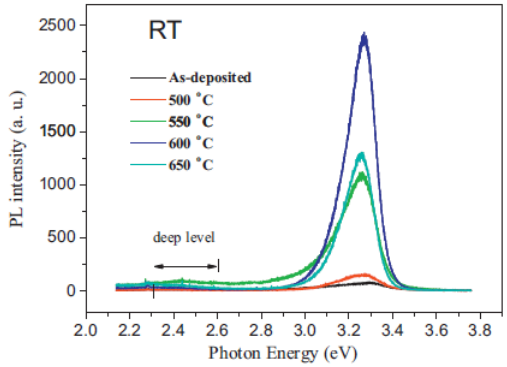

Fig. 3. RT-PL spectra of ZnO films: as-deposited and post-annealed at different temperatures.

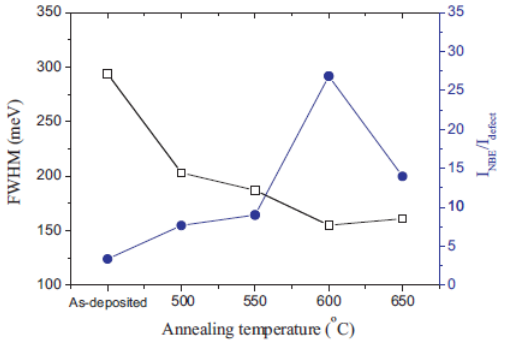

Fig. 4. Variation of $I_{NBE}/I_{deep\text{-}level}$ ratio and FWHM of RT-PL spectrum as a function of post-annealing temperature. The data from the as-deposited sample is also given for comparison.

increase of annealing temperature to 650 °C makes the hole concentration decrease. The reduction of hole concentration may be due to the enhanced interdiffusion of Ga atoms to form the donors of Ga_{Zn}, which induce the carrier compensation phenomenon. Moreover, as the annealing temperature is increased from 500 to 650 °C, the mobility of film monotonously decreases as shown in Fig. 2. This is probably due to that both As and Ga atoms introduced into the ZnO grown film not only contribute to the carrier generation but also introduce the scattering effect on carriers, which therefore reduces the Hall mobility. The reproducibility of the post-annealing effects on p-type conductivity has been recognized for the specimens both from the same wafer and from different growth runs. It should be mentioned that the electrical properties of all the fabricated films have been measured again 30 days later and the stability of electrical properties have been confirmed.

The PL measurements were performed to investigate the influence of annealing temperature on the optical properties of ZnO thin film. Fig. 3 shows the room-temperature PL spectra (RT-PL) of the as-deposited film and those annealed at 500, 550, 600, and 650 °C, respectively. Obviously, the PL results are strongly dependent on the annealing temperature. Both the as-deposited specimen and that annealed at 500 °C exhibit relatively weak near-band-edge (NBE) emissions around 3.291 and 3.278 eV, respectively. However, as the annealing temperature is increased to 550 °C and above, the NBE emission around 3.26 eV intensifies greatly with the intensity arriving at the maximum for the film annealed at 600 °C. This result indicates that the film quality has been improved by elevating the temperature to 550 °C and above for post-annealing treatment. Even an excess structure of Zn_3As_2(1 1 1) is demonstrated in the XRD result, the optical property of films seems not to deteriorate. Fig. 4 gives a more clear comparison between the RT-PL spectra obtained. Here, the intensity ratio of NBE emission and deep-level emission ($I_{NBE}/I_{deep\text{-}level}$) as well as the full width at half maximum (FWHM) of NBE emission is plotted as a function of annealing temperature. As shown, the FWHM of RT-PL for the film annealed at 600 °C demonstrates a lowest value of 155 meV. Also, the $I_{NBE}/I_{deep\text{-}level}$ ratio increases with increasing annealing temperature and exhibits the maximum for the film annealed at 600 °C. However, it decreases again with increasing annealing temperature further, which implies that some excess defects are produced in the film when the annealing is carried out at a temperature high to 650 °C. Possible causes of these defects include the decomposition of ZnO film and too many interdiffused As and Ga atoms, which lead to the formation of structural defects causing the deep-level emission [20]. Clearly, the results of RT-PL are in good agreement with those obtained from XRD and Hall analyses.

To investigate further the optical properties and detailed luminescence mechanisms of films, low temperature PL (LT-PL) measurements were performed at 10 K and the results are collected in Fig. 5. As shown in Fig. 5(a), the LT-PL spectrum of the

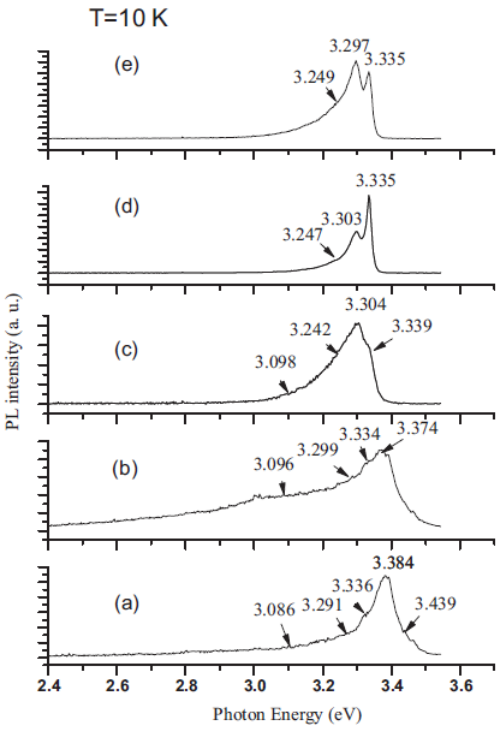

Fig. 5. LT-PL spectra of (a) as-deposited film and those post-annealed at temperatures: (b) 500, (c) 550, (d) 600, and (e) 650 °C.

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as-deposited specimen exhibits five emission lines at 3.439, 3.384, 3.336, 3.291, and 3.086 eV, respectively. The lines at 3.384 and 3.439 eV are assigned to the first ($n=1$) and the second ($n=2$) excited state transitions of free exciton (FX), respectively [21]. The presence of emissions originated from free excitons might manifest the good quality of film produced. Furthermore, the line at 3.336 eV has been identified as a neutral acceptor bound exciton (A^0X) [14,22] and those at 3.291 and 3.086 eV are assigned to the free electron to neutral acceptor (FA) transition [22,23] and zinc vacancy (V_{Zn}) related emission [24], respectively. These features suggest that the As atom-related acceptors and native defect of V_{Zn} exist in the as-deposited film to induce the p-type conductivity therein. On the other hand, the LT-PL spectra from the specimens conducted with the post-annealing are displayed in Figs. 5(b)–(e). For the specimen post-annealed at 500 °C, the spectrum is still dominated by the line at 3.374 eV related to FX [25] except that the relative magnitude is much reduced. Namely, both the A^0X and FA lines specified for the as-deposited specimen intensify with increasing annealing temperature and situated at 3.334–3.339 and 3.297–3.304 eV, respectively. These two peaks even dominate the whole PL spectrum for the specimens post-annealed at temperatures of 550 °C and above. In particular, as shown in Fig. 5(d), the dominance of a sharp A^0X peak is evident for the spectrum of the film post-annealed at 600 °C. This result associated with that the same specimen has demonstrated the highest hole concentration in previous Hall measurement suggest the superior quality of p-type film has been achieved. Else, the lines situated at energies ranging from 3.242 to 3.249 eV in Fig. 5(c)–(e) are suggested to be induced by the donor–acceptor pair (DAP) recombination [14,23]. It is also worth noting that the intensity of A^0X emission is reversed by that of FA emission for the sample post-annealed at 650 °C. This is considered to be due to the introduction of excess Ga elements, which are easy to become donors in ZnO film, dissociating the A^0X and therefore enhancing both FA and DAP recombination simultaneously. The acceptor energy of As-related dopant can be estimated by [22,23]: $E_A = E_g - E_{FA} + k_BT/2$, where E_g is the intrinsic band gap and E_{FA} the emission energy released by the free electron-acceptor level transition. Using $E_g = 3.437$ eV reported elsewhere [25] and the values specified in the PL spectra for E_{FA}, the value of E_A is estimated to be 133–146 meV. This value is in good agreement with theoretical ionization energy of 150 meV predicted for the $As_{Zn}–2V_{Zn}$ complex [11] as a shallow acceptor in ZnO. Although the microstructures with Zn_3As_2 phase exhibited for the post-annealed samples are also likely to be the origin of p-type conduction, the corresponding activation energy is high to about 930 meV [26]. Therefore, the doping mechanism of the present p-type ZnO film should be much more possible to be the formation of $As_{Zn}–2V_{Zn}$ complex. Here, the As atom is being substituted for Zn site to act as a donor, but is accompanied by two Zn vacancies to have a net effect of supplying one hole per complex defect [11].

As indicated by the XRD analyses, the post-annealing conducted at different temperatures result in the interdiffusion of As and Ga atoms across the ZnO/GaAs interface with different degrees. The diffusion of As atoms into ZnO film is favorable for forming $As_{Zn}–2V_{Zn}$ complex therein. However, the diffusion of Ga atoms into ZnO film is also inevitable, which will result in the compensation effect on doping. The post-annealing treatment performed at 600 °C is thus suggested to have the interdiffused arsenic atoms form $As_{Zn}–2V_{Zn}$ complex quite effectively, which therefore induced the highest p-type conductivity and the superior film quality.

4. Conclusions

Stable p-type ZnO films can be fabricated on semi-insulating GaAs substrate by AP-MOCVD using DEG and H_2O as the source precursors and a gas flow ratio of $[H_2O]/[DEG] = 3.42$. The hole concentration of the as-deposited film is 3.22×10^{18} cm^{-3}, while that of the specimens post-annealed at 500–600 °C ranges from 4.7×10^{18} to 8.7×10^{19} cm^{-3}. The doping mechanism for the p-type ZnO films obtained is suggested to be the formation of $As_{Zn}–2V_{Zn}$ complex. Conclusively, the interdiffusion of As and Ga atoms across the ZnO/GaAs interface is enhanced by the post-annealing treatment. In particular, the post-annealing treatment conducted at 600 °C is found to be beneficial for obtaining the superior-quality p-type ZnO film.

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論文摘要集

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電質屏蔽放電管之先期研究

*徐銘鎧　魏碧玉　徐仁宏
工業技術研究院材料與化工研究所

屏蔽放電(dielectric barrier discharge)又稱為無
技術是產生高能電子的有效方法，能在較低的
化學反應所需的活性粒子。本研究主要探討充
電質屏蔽放電管於不同氣體壓力時，其放光強
光譜之差異，由於氙氣 DBD 放發管的光譜主要
147nm、150nm、173nm、823nm 及 828nm 此
其中 147nm、150nm 及 173nm 屬於真空紫外線
在 PL 的量測上實屬不易，因此本研究之 PL
討論波長為 823nm 及 828nm 的相對強度與
管光照度之關係。實驗結果顯示此氙氣 DBD 放
真壓力為 400torr 左右時有最佳之光照度，而 PL
波長 823nm 與 828nm 的相對強度比值範圍在
之間也會得到最佳之光照度。

電質屏蔽放電、無聲放電、準分子燈、微放電

雜元素於氧化鋅奈米線結構及其光學特性之研究

霖[1]　陳宏仁[1]　高銘政[1]　林宸澈[2]　貢中元[2]
平技術學院電子工程系 [2]中興大學電機工程系
(NSC99-2112-M-164-001)

究主要在探討不同的摻雜元素對於氧化鋅(Zn
$A_{0.02}O$, A=Cu, Sm)本體結構之螢光發光特性以
之變化探討。經過 X-ray 繞射分析證實樣品具有
02)優選取向，且無二次相產生。利用場發射式電
微鏡觀察到利用簡單的液相沉積法可以製備出
米線陣列，其奈米線線徑會隨著摻雜元素不同而
。螢光光譜分析可以得到 UV 光的部分會隨著摻
有減弱的趨勢，而在可見光的部分則是因為氧空
而有發光增強的現象。磁性量測可以得到飽和磁
別為 ZnO (0.102 emu/g)、$Zn_{0.98}Sm_{0.02}O$ (0.128
$Zn_{0.98}Cu_{0.02}O$ (0.042 emu/g)。

氧化鋅、螢光光譜、奈米線、鐵磁性

04-0650

Improving the efficiency of multicrystalline silicon solar cells by using phosphorus diffusion gettering

*Sz-Tseng Wu (吳思增)[1], Heng-Wei Lin (林政緯)[1], Shan-Ming Lan (藍山明)[1], Wu-Yih Uen(溫武義)[1], Tsun-Neng Yang(楊村農)[2], Jian-Wun Chen(陳建文)[2], Yu-Han Su(蘇郁涵)[2], Yu-Hsiang Huang(黃昱翔)[2], Jin-jhan Jheng(鄭金展)[2],Chin-Chen Chiang(江金鎮)[2]

1. Department of Electronic Engineering, Faculty of Engineering, Chung Yuan Christian University
(中原大學 電子工程系)
2. Institute of Nuclear Energy Research
(行政院原子能委員會核能研究所)

This study will discuss the effect of removal of harmful impurities such as Fe, Co and Ni, etc by adding phosphorous diffusion gettering (PDG) in mc-Si solar cell processes. We believe that the procedure can reduce the internal carrier recombination rate and increase the minority carrier lifetime, further improve the conversion efficiency of solar cells. The minority carrier lifetime measurement is performed using the microwave-reflection photo-conductance-decay (MRPCD) technique, which is capable of determining the lifetime of a silicon wafer. We also used the secondary ion mass spectrometry (SIMS) to observe the distribution of metal impurities near silicon surface after PDG. It shows an increasing in the minority carrier lifetime from 24.3us to 45.6us, and conversion efficiency was improved about 2% for PDG treatment.

Keyword: PDG, silicon solar cell, lifetime, mc-Si

04-0657

利用電泳沉積法與機械壓縮技術應用於可撓式染料敏化太陽能電池

閔庭輝[1]、*洪志豪[2]、趙時勉[3]、陳維婷[2]、蔡振凱[1]、劉育松[1]、吳添全[1]、柯智揚[1]、黃建榮[4]
Teen-Hang Meen[1], Jhih-Hao Hong[2],Shi-Mian Zhao[3],Wei- Ting Chen[2], Jenn-Kai Tsai[1],Yu-Sung Liu[1],Tian-Chiuan Wu[1], Zhi-Yang Ke[1], Chien-Jung Huang[4]
(NSC-98-2622-E-150-001-CC1)、(NSC-98-2221-E-150-003)

[1]國立虎尾科技大學電子系
[1]Department of Electronic Engineering, National Formosa University, Yunlin 632, Taiwan
[2]國立虎尾科技大學光電與材料科技研究所
[2]Institute of Electro-Optical and Materials Science, National Formosa University,Yunlin 632, Taiwan

[3]修平技術學院電機
[3]Department of Electrical Engineering, Technology, Taichung County
[4]國立高雄大學應用物
Department of Applied Physics, National Nan-Tzu, Kaohsiung 811

本論文是利用電泳沉積法製備二
機械壓縮技術，研究二氧化鈦電極
膜結構以及電池元件特性之影響。由
所發現，電泳沉積法製備二氧化鈦
有利於更多染料的吸附，顆粒大小
可以使薄膜結構更緻密，電子傳輸
發現，二氧化鈦電極結晶相為銳鈦
壓縮製程而有所改變，在太陽光
下，壓縮後之薄膜最佳效率由 1.91

關鍵字：可撓式、電泳沉積法

04-0662

Zn_2SiO_4摻雜Al、Sc與摻
薄膜性質研

*謝庚霖[1]　彭坤增[1]　侯明
[1]明志科大材料工程學系　[2]國立臺灣

氧化鋅薄膜結構為纖鋅六方
晶面優選取向。本實驗Zn_2SiO_4摻
色螢光薄膜，薄膜在1200℃熱處
料的發光亮度和效率提高，熱處
性，更降低Quartz與鍍層間界面(
摻雜Al-Sc經1200℃燒結相較於1
面張力的影響而呈現顆粒分散，
圖譜分析知結構由ZnO相轉成α-
加由 53.75 nm 增加至 84
PL(photoluminescence)呈現出線
1000℃退火後摻雜不同元素並
現；然而，其基材中並未發現摻
訊號。在1100℃退火後，ZnO
強度增加，鍍膜的結晶性變得較
的關係。

關鍵字：α-Zn_2SiO_4；Zn_2SiO_4摻
差

翻製

魏茂國[1] 林宏鼎[1]
術學院土木工程系
所
2-E-259-001-CC3)

IS/石英玻璃複合
面光罩對準機翻製
時間與不同黏度的
發現，當接觸時間
出的 PMMA/PU
黏度的紫外線硬化
於低黏度的紫外

形

翻製

劉育豪[1] 魏茂國[1]
[1] 大漢技術學院土木
所
E-259-001-CC3)

製作出奈米結構，
製程研究當中，
膜表面結構的週
，我們也發現了
。而翻模製程實
30 wt%、真空
後 GST 薄膜表

反射效應

浩[2] 魏茂國[1]
灣大學光電工程

59-003, NSC 98-

(ITO)/ 3,
tyrenesulfonate

PEDOT: PSS) (20 nm)/ copper phthalocyanine (CuPc) (20 nm)/ fullerene (C_{60}) (40 nm)/ bathocuproine (BCP) (7 nm)/ Ag (100 nm) 之小分子有機光伏（organic photovoltaic，OPV）元件為基礎，設計實驗並探討元件中多重反射效應（multiple reflection effect）。從光電流密度的變化中，我們可以發現此效應與入光面積、位置與角度有關。入光面積影響光電流密度約為單位面積(mm^2) 0.8 mA/cm^2；隨入光位置而遞減，其變化幅度約在 μA/cm^2；入射角度變化在 65°達到峰值約 800 μA/cm^2。

關鍵字：有機光伏(OPV)、多重反射

04-0961

含噁二唑團基之電子輸送材料

*蔡成章[1] 李泰興[1] 丁永強[2] 楊先仁[1] 吳知易[3]
[1]大葉科技大學材料科學與工程學系 [2]遠東科技大學化妝品應用與管理系 [3]崑山科技大學綠色材料所

本研究合成一系列主鏈含噁二唑(1,3,4-oxadiazole, OXD)團基與不同脂肪長度之聚醚(**PO5-PO10** and **PO12**)。將含噁二唑團基的高分子**PO7**當成製作PLED元件的電子輸送層，摻雜於含三鍵全共振的發光高分子(**P7**)中，發現此系統的主要發光是長波長，並且能量很有效率地從**PO7**的噁二唑鏈段轉移到**P7**的PPEF主鏈上。噁二唑鏈段增加雜系統的電子親和力可降低LUMO能階，而所有的摻雜系統之雙層PLED元件都發射黃光。由於噁二唑團基具有電子特質可提高電子注入發光層的速率，平衡電荷的注入，增加發光效率。因此，添加適量的**PO7**可使降低元件起使電壓並且提高最大亮度，

關鍵字：噁二唑、電子輸送材料、 PLED 元件

04-0968

奈米結構化氧化鋁鋅薄膜之製作與光電性質研究

董彥廷(Yen-Ting Tung)，蔡睿翰(Ruei-Han Tsai)，張宏臺(Hung-Tai Chang)，李勝偉(Sheng-Wei Lee)*
Institute of Materials Science and Engineering, National Central University
(國立中央大學 材料科學與工程研究所)
(NSC 97-2221-E-008-091-MY3)

本研究利用溶膠凝膠技術搭配旋轉塗佈法製備氧化鋅(ZnO:Al)薄膜，藉由摻雜鋁離子來探討其摻雜濃度對膜之光、電特性影響。實驗結果顯示當鋁摻雜濃度為 1 % 薄膜擁有最低之片電阻值，且隨著摻雜濃度的提升其光吸收限有藍位移之趨勢(Burstein-Moss 效應)。此外研究中亦嘗試將氧化鋁鋅薄膜旋塗於不同蝕刻秒數之矽基奈米柱陣列上並施以熱處理，經由光反射率及光激發螢光之量測可得知當矽基材蝕刻秒數增加，薄膜之螢光強度亦隨著增強，此現象證實了矽基材之結構愈粗糙，薄膜愈能有效地降低光反射並使光吸收量增加。

關鍵字：氧化鋁鋅、溶膠凝膠法

04-0970

非極性氮化鎵於圖案化藍寶石基板上之成長

*莊樹瑋[1] 田志盛[2] 王尉霖[2] 林博文[2] 張立[2] 吳耀銓[2] 張翼[2]
[1]國立交通大學工學院半導體材料與製程設備學程 [2]國立交通大學材料科學與工程學系
(98-EC-17-A-07-S2-0045)、(NSC98-2221-E-009-042-MY3)

本研究利用金屬有機化學氣相沉積製程系統(MOCVD)於圖案化藍寶石基板(Patterned Sapphire Substrate, PSS)上成長非極性氮化鎵磊晶膜。改變磊晶製程參數藉由 XRD、SEM 與 TEM 探討氮化鎵與圖案化藍寶石基板磊晶關係。由實驗結果可知其磊晶成長機制與氮化鋁(AlN)有極密切關係，當使用低溫製程的氮化鋁(AlN)當緩衝層時其氮化鎵在成長時偏向於磊晶側向成長(Epitaxial Lateral Overgrowth, ELO)，進而可成功的於 A 面圖案化藍化藍寶石上成長出 M 面非極性氮化鎵磊晶，其 X-ray rocking curve 半高寬(FWHM) ~600arcsec。

關鍵字：氮化鎵(GaN)、金屬有機化學氣相沉積(MOCVD)、圖案化藍寶石基板(PSS)

04-0973

研製高效率PERL(passivated emitter, rear locally-diffused)單晶矽太陽能電池

*Li-Wei Zeng (曾立偉), Heng-Wei Lin (林政緯)1, Shan-Ming Lan (藍山明)1, Wu-Yih Uen(溫武義) 1,
Tsun-Neng Yang(楊村農) 2, Jian-Wun Chen(陳建文) 2, Yu-Han Su(蘇郁涵) 2, Yu-Hsiang Huang(黃昱翔) 2,
Jin-jhan Jheng (鄭金展) 2, Chin-Chen Chiang(江金鎮) 2
1. Department of Electronic Engineering, Faculty of Engineering, Chung Yuan Christian University
(中原大學電子工程學系)
2. Institute of Nuclear Energy Research
(行政院原子能委員會核能研究所)

因全面積鋁膠網印在燒結之後會形成鋁矽合金層，造成缺陷的產生與表面的不平整，使得電池表面復合速率升

Improving the efficiency of multicrystalline silicon solar cells by using phosphorus diffusion gettering

＊Sz-Tseng Wu (吳思增)[1], Heng-Wei Lin (林政緯)[1], Shan-Ming Lan (籃山明)[1], Wu-Yih Uen(溫武義)[1], Tsun-Neng Yang(楊村農)[2], Jian-Wun Chen(陳建文)[2], Yu-Han Su(蘇郁涵)[2], Yu-Hsiang Huang(黃昱翔)[2], Jin-jhan Jheng(鄭金展)[2],Chin-Chen Chiang(江金鎮)[2]

1. Department of Electronic Engineering, Faculty of Engineering, Chung Yuan Christian University (中原大學 電子工程系)

2. Institute of Nuclear Energy Research (行政院原子能委員會核能研究所)

This study will discuss the effect of removal of harmful impurities such as Fe, Co and Ni, etc by adding phosphorous diffusion gettering (PDG) in mc-Si solar cell processes. We believe that the procedure can reduce the internal carrier recombination rate and increase the minority carrier lifetime, further improve the conversion efficiency of solar cells. The minority carrier lifetime measurement is performed using the microwave-reflection photo-conductance-decay (MRPCD) technique, which is capable of determining the lifetime of a silicon wafer. We also used the secondary ion mass spectrometry (SIMS) to observe the distribution of metal impurities near silicon surface after PDG. It shows an increasing in the minority carrier lifetime from 24.3us to 45.6us, and conversion efficiency was improved about 2% for PDG treatment.

Keyword: PDG, silicon solar cell, lifetime, mc-Si

Introtuction

The main advantages of cast multicrystalline silicon material are prepared by low energy consumption and low cost. However, the drawback is that the grain boundary contains a high density of impurities and dislocations, which affect the conversion efficiency of multicrystalline silicon solar cells. The main reason is the cast multicrystalline silicon containing a high concentration of deep level impurities such as iron, cobalt, nickel and other metal impurities. These harmful impurities will become the minority carrier recombination centers so that the minority carrier lifetime decreases, and further affects the conversion efficiency. Owing to a lot of harmful impurities containing in multicrystalline silicon substrates, an additional extrinsic gettering process is performed for removing any gettered impurities. In this, we will be considered the gettering mechanisms such as phosphorous diffusion gettering (PDG) [1].

After gettering processes, through the surface texturing, $POCl_3$-diffusion, SiN_x anti-reflection coating screen printing of Al-paste and Ag-paste, electrical isolation, I-V measurement will also be intergraded into cell fabrication. Photovoltaic conversion efficiency will be increased. Therefore, This fabrication technique of gettering is possible to reduce the cost of silicon solar cells since only a thin film of material is used.

Experiment

The mc-Si substrate was provided from “Green

Energy Technology", with bulk concentration of $2.8\times10^{17}cm^{-3}$, resistivity of 0.67Ω-cm, thickness of about 200~220μm, grain size of 0.5~1cm. The area of solar cell is $1x1cm^2$.

Before gettering, there are some important works to clean up silicon wafers. First, in order to remove dust and organic particles, silicon wafers were cleaned in trichloroethylene (TEC) and acetone (ACE) in ultrasonic cleaner each for 3 min. the saw damage removed by 20% KOH (weight%) alkaline etching solution at a temperature of 75°C.

Phosphorus diffusion gettering(PDG) was used in our experiments. The gettering region near the surface was phosphorous diffused at 870℃ for 40 min which resulted in a sheet resistance of 33.5 Ω/□, and a junction depth of approximately 0.3 μm [2]. After $POCl_3$-diffusion, a post annealing process is performed to attract metal impurities with the various annealing temperatures and times. After PDG, the wafers could then be surface etched in suitable chemical solution(KOH 20 wt.% at 75℃) to remove the gettering layer [3].

To create an n^+-p junction, here we choose a three-zone furnace as $POCl_3$ diffusion furnace. Before screen-printing of Al-paste, wafers were dipped in HF dilute solution to remove SiO_2 film. Aluminum- paste was screen-printed on the backside and dried at 150℃. Next, the aluminum alloyed back surface field (BSF) was formed in a I-R furnace.

Metal mask was used to define front metal contact patterns. Titanium (500Å), palladium (700 Å), and sliver (7000Å) were sequentially deposited by electron beam evaporation to form the multilayer metal contact patterns. After that, wafers were sintered in hydrogen ambiance at 450°C.

The antireflective coating (ARC) is one of the most important parts of solar cell fabrication. In this work, SiNx was deposited by plasma enhanced chemical vapor deposition system(PECVD). The film thickness is approximately 800Å [4]. A schematic diagram of mc-Si solar cell structure is shown in Fig. 1.

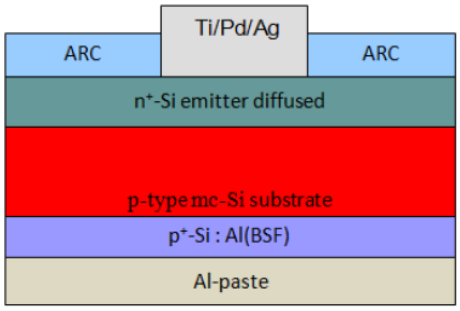

Fig. 1 The mc-Si solar cell structure.

Results and Discussion

Lifetime measurement

The minority carrier lifetime measurement is performed using the microwave reflection photoconductance decay (MR-PCD) technique [5,6], which is capable of determining the lifetime of a silicon sample after $POCl_3$ diffusion at 870℃ for 40min, which resulted in a suitable sheet resistance of 63.6 Ω/□ for n-p junction.

The results are shown in the Table 1. Comparing the histograms before and after post annealing, the minority carrier lifetime of A-2 is clearly improved to higher than as-grown. In the low-temperature condition of 700℃, the lifetime measurement has a more significant result especially. The low-temperature post annealing improve the result of gettering. This is related to two main effects: depletion of precipitates, and improvement of segregation ratio to the gettering layer [7]. Since PDG is segregation-type gettering, the concentration enhancement of impurities in phosphorus-diffused layers is increasing with low-temperature post annealing [8,9].

In order to remove the gettered region completely, effect of etching time on minority carrier

lifetime was considered. Table .1 and show the results in the lifetime as changes of etching time clearly. From the results of etching time for 7.5 min and 10min, the mc-Si substrate may be too thin to induce the higher surface recombination velocity.

Table 1. The values of minority carrier lifetime of A-1~A-4 were measured with different etching time by MR-PCD.

Experimental number \ Etching time	5 (min)	7.5 (min)	10 (min)
A-1($POCl_3$ diffusion 870℃ 40min, no post annealing)	26.2us	23.1us	20.4us
A-2($POCl_3$ diffusion 870℃ 40min, post annealing 700℃ 100min)	41.2us	39.4us	35.1us
A-3($POCl_3$ diffusion 870℃ 40min, post annealing 870℃ 100min)	31.9us	27.4us	21.1us
A-4($POCl_3$ diffusion 870℃ 40min, post annealing 980℃ 100min)	16.5us	15.9us	11.4us

In the each experiment with different post annealing time, the measured minority lifetimes are shown in Table 2.The effective lifetime is improved from 24.3μs for as-grown to 45.6μs for the sample B-5 with etching time for 5 min [10]. Longer gettering at a standard temperature may also result in an increase in the conversion efficiency [7]. During long-time post annealing, impurities could be attracted into the traps effectively so that the purity of mc-Si substrate was improved after the gettering region removing.

Table 2. The values of minority carrier lifetime of B-1~B-5 were measured with different etching time by MR-PCD.

Experimental number \ Etching time	5 (min)	7.5 (min)	10 (min)
B-1($POCl_3$ diffusion 870℃ 40min, no post annealing)	26.2us	23.1us	20.4us
B-2($POCl_3$ diffusion 870℃ 40min, post annealing 700℃ 25min)	30.7us	28.9us	24.3us
B-3($POCl_3$ diffusion 870℃ 40min, post annealing 700℃ 50min)	33.5us	30.1us	25.1us
B-4($POCl_3$ diffusion 870℃ 40min, post annealing 980℃ 100min)	41.2us	39.4us	32.0us
B-5($POCl_3$ diffusion 870℃ 40min, post annealing 700℃ 200min)	45.6us	42.0us	33.7us

Conversion efficiency and I-V data for solar cells

The I-V characteristics with increases in post annealing time at 700℃ are shown in Fig.2. The conversion efficiency was much increased by adding a post annealing process, while the long-time post annealing improves the conversion efficiency more effectively than no post annealing in PDG processes. The best cell is B-5 with etching time for 5 min, which parameters are: open-circuit voltage of 595 mV, short-circuit current of 32.57 mA, fill factor of 73%, and efficiency of 14.18%.As demonstrated in both lifetime and I-V results described above, the diffusion effects of impurities toward the gettering region can be enhanced in an increase of post annealing time.

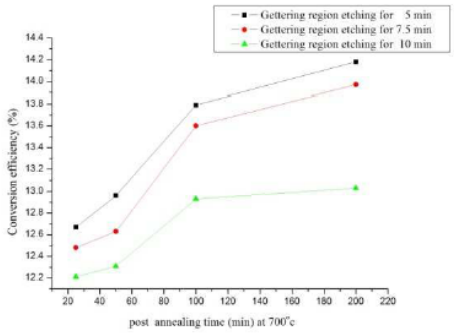

Fig. 2 Different post annealing time at 700℃ vs. conversion efficiency with different etching time.

SIMS measurement of the impurities

SIMS depth-profiling measurements done from the front surfaces of the mc-Si wafers showed that the gettering treatment caused impurities in the bulk of the wafers to diffuse and precipitate at the phosphorous diffused region.

The SIMS depth profiles of the Ni impurity concentration are shown in Fig.3. The distribution of Ni impurity concentration near the surface is no significant increasing with PDG processes. However, the gettering effect of sample B-5 on Ni impurity is more effectively than A-4.

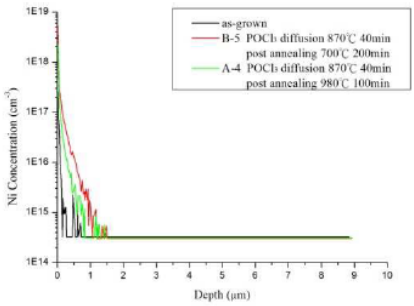

Fig.3 SIMS depth profiles of the Ni impurity.

Conclusions

This experiment showed that phosphorous diffusion gettering can be used as a getter agent for unwanted impurities in mc-Si wafers. We observed the best post annealing temperature is at 700℃ for 200min after $POCl_3$ diffusion at 870℃ for 40min. Under this condition, impurities were diffused effectively to the defect region and were trapped. The average minority carrier lifetime of wafers increased from 24.3 μs for as-grown to 45.6 μs for sample B-5 due to a reduction of internal minority carrier recombination by phosphorous diffusion-induced impurity gettering.

A relationship between minority carrier lifetime and conversion efficiency is observed in this study. The I-V characteristic of mc-Si was shown to be improved an increase in a relatively high efficiency of 14.18% for the sample B-5. As shown in the results of SIMS measurement, the gettering effects were observed for the detrimental impurity Ni. The Ni impurity concentrations are lower than as-grown sample. Reduction of metallic impurity in the mc-Si bulk is a reason that the minority carrier lifetime and conversion efficiency can be improved.

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研製高效率 PERL(passivated emitter, rear locally-diffused)單晶矽太陽能電池

＊Li-Wei Zeng (曾立偉), Heng-Wei Lin (林政緯)[1], Shan-Ming Lan (籃山明)[1], Wu-Yih Uen(溫武義)[1], Tsun-Neng Yang(楊村農)[2], Jian-Wun Chen(陳建文)[2], Yu-Han Su(蘇郁涵)[2], Yu-Hsiang Huang(黃昱翔)[2], Jin-jhan Jheng (鄭金展)[2], Chin-Chen Chiang(江金鎮)[2]

1. Department of Electronic Engineering, Faculty of Engineering, Chung Yuan Christian University
(中原大學 電子工程學系)
2. Institute of Nuclear Energy Research
(行政院原子能委員會核能研究所)

利用常壓式有機金屬物化學氣相沈積法（APMO-CVD）沉積氧化鋁可以有效降低生產成本，再利用 PERL(passivated emitter, rear locally-diffused)技術可以有效提高單晶矽的太陽能轉換效率，此技術有背面鈍化效果，並可以增加少數載子壽命。我們將未經過 PERL 技術處理的太陽能電池元件與有使用 PERL 技術的太陽能電池元件比較，有做 PERL 其太陽能轉換效率可達 12.4%，氧化鋁薄膜成長最佳條件為 450℃、10 分鐘。

關鍵字：PERL、Al_2O_3、太陽能電池、常壓式有機金屬物化學氣相沈積法

1. 前言

近年來世界各地的科學家一直在尋找合適的技術生產矽原料的光電產業及原料並滿足需要"低成本"，以及是否需要足夠的質量。其中以單晶矽(sc-Si)與複晶矽(mc-Si)作為基板的太陽能電池應用最為廣泛，占太陽能電池產業的 90%左右，現今製作單晶矽太陽能電池基板的方法，大部分是利用西門子製程法來得到高純度的單晶矽棒，再經線切割成為(厚~200μm)基板，之後經絨面、磷擴散、電性阻絕、鍍抗反射層和電極製作等程序，而形成單晶矽太陽能電池。

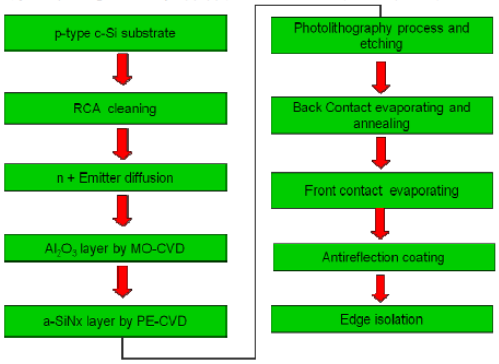
但因為背電極以鋁膠網印燒結之後，會產生 Al-Si 合金層，對此造成的缺陷與表面的不平整會使得電池背部表面複合效率提高，且全區域網印也會降低了晶片的內部反射以至於影響電池的背面光吸收 [1] [2]。

PERL(passivated emitter, rear locally-diffused)技術除了可以將表面鈍化改善表面複合速率，並利用介電層如二氧化矽（SiO_2）、氧化鋁（Al_2O_3）等成長於基板背面，開窗之後鍍上金屬電極，而氧化層介於矽基板的中間，一方面可以增強背面光吸收，以增強矽基板對長波長的吸收，另一方面，經低溫回火後也可降低背表面 p 型區域的複合速率 S，進而有效的改善電池的電流收集效益 [3] [4]。

本研究是利用常壓式有機金屬物化學氣相沈積法沉積氧化鋁在 p-type 基板的背面上，主要是因為氧化鋁有幾種特性，氧化鋁在特定材料源(如副產物帶有氫氣)在低溫成長時，可使材料帶有一定的氫含量(~ 3 at.%)，低溫回火後對於鈍化基板表面懸浮鍵有一定的效果，同時，此材料在與基板接面處(Si-Al_2O_3)會帶有內建負電荷(Qf= 10^{10}~10^{12} cm^{-2})，可應用在太陽能電池的 p 型區域上，可加強少數載子電動流的收集。而氧化鋁也是一種寬能隙(~9 eV)的介電材料，因此在可見光波段不易被吸收，光穿透性佳，與金屬電極之間再結合 SiO_2 薄膜(p-type c-Si/Al_2O_3/SiO_2/Al)，能再增強背面光吸收 [5] [6]。

2. 實驗方法

本次所選用的基板為購自中美矽晶公司的 p-type c-Si 晶片，其電阻係數約為 1Ω-cm，經由 PERL 技術形成太陽能電池結構圖與其大致上的流程如圖一所示：



圖一、PERL 矽太陽能電池製作過程

在 p-type c-Si 基板經過 RCA 標準清洗步驟，完成晶片清洗後，接著製作射極層使之與主動層形成之 pn 接面，來提供內建電場，並未有吸收光能之功用，所以在製作時以厚度薄為主要目標，避免光在尚未到達 pn 接面時，就被射極層所吸收。

製作 n^+-Si 射極層時，首先將 p-type c-Si 晶片置入加熱爐管中，進行磷原子(P)擴散。製程中 P 原子的材料源為液態之 $POCl_3$，在 $POCl_3$ 液體中，通入氮氣當作承載氣體，將 $POCl_3$ 帶入反應腔中，並與另外通入的氧氣進行反應，使其生成 P_2O_5，然後再與 p-Si 主動層表面反應，生成 P 原子與 SiO_2 膜，最後 P 原子再經由熱擴散進入主動層中，形成 n^+-Si 層，最後 SiO_2 膜以稀釋氫氟酸(HF:H_2O=1:10)蝕刻去除；而一般於太陽能電池的結構上，pn 接面照光後會產生少數載子電子、電洞流，由於內建電場的驅使下，會使電子往 n 型區域擴散，而電洞往 p 型區域擴散，而 p 型區域上帶負電荷的氧化鋁，可以對入射陽光所產生的少數載子電洞提供有效的吸引作用，進而提高短路電流，增加轉換效率。

本次實驗利用常壓式有機金屬物化學氣相沉積(APMO-CVD)系統進行，Al_2O_3 成長步驟如(A)與(B)所

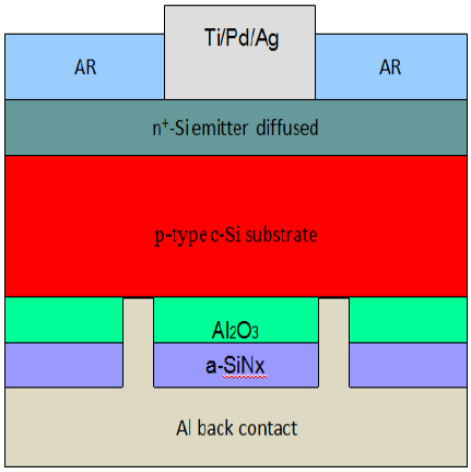
示。其中 Al_2O_3 的氣體材料源為 alternating trimethylaluminium(TMA)與水 (H_2O)，承載氣體為氮氣。(A)成長前腔體熱處理，於 HCl+H_2 混合氣體中以1225℃烘烤數分鐘，目的在於去除腔體內和石墨中殘餘雜質。(B)沉積 Al_2O_3 介電層，成長溫度： 450℃，時間：10-20 分鐘。

接著在氧化鋁薄膜上沉積可增加背面光吸收之材料，本計畫將選用氮化矽(SiN_x)，其折射係數 n=2，可利用電漿輔助化學氣相沉積(PECVD)系統成膜。

電極孔洞之製作是在介電層 a-SiNx 上以旋轉塗佈機佈上負阻，在軟、硬考之後，在使用設計之光罩(面積為 80nm x 80nm，孔洞間距 1000 μm，直徑為 100~200 μm)曝光，而後顯影，再以稀釋氫氟酸(HF:H_2O=1:10)蝕刻介電層(a-SiNx、Al_2O_3)形成接觸孔洞 [7]。

正電極(front contact layer)以本研究所研製之磊晶矽太陽能電池將使用 Ti/Pd/Ag 金屬當正電極，其理由如下：由於鈦(Ti)功函數低，有抵抗溼氣的功用，並且會增加金屬與 Si 的附著力，與 Si 會形成良好的歐姆接觸電極，銀(Ag)為低電阻的材料，鈀(Pd)可防止 Ti 和 Ag 反應，而 Pd 和 Ag 之組合亦有降低串聯電阻的功用。另外，我們會將 Ti/Pd/Ag 金屬做成柵狀電極，減少金屬線遮蔽入射光的比例。

背電極(back contact layer)因為不用考慮到是否影響光吸收的問題，所以可選擇導電性良好的金屬，直接將金屬以電子束蒸鍍機鍍在基板上形成一層金屬膜(Al)，再藉由回火，使其與基板形成歐姆接觸。再採用採用氮化矽(a-SiNx)作為抗反射層。PERL 矽太陽能電池結構如圖二所示。



圖二、PERL 矽太陽能電池結構圖

3.結果與討論

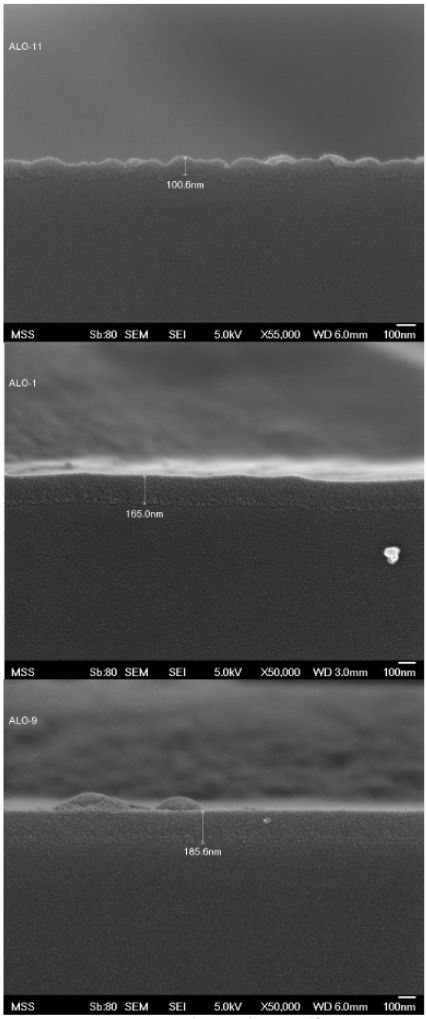
實驗結果如表一所示，先用基本製程用磷擴散作 n-p 介面，再做正反電極但未在背面沉積氧化鋁薄膜作為介電層所做的太陽能電池元件當作基準片，其 I-V 量測太陽能轉換效率為 10.44%。接著再利用前述的實驗方法將氧化鋁薄膜沉積於 p 型基板背面，其轉換效率為 12.4%，我們可以明顯的發現其轉換效率比未做 PERL 技術多了接近 2%的。由此結果我們可以證實了氧化鋁薄膜沉積在 p 型基板背後確實有鈍化效果，並增加了少數載子的壽命，降低表面複合速率，所以太陽能轉換效率才有顯著提升。

表一、在 AM=1.5 下，I–V 量測太陽能電池轉換效率

	Voc (V)	Isc(mA)	Pm(mW)	FF(%)	Eff(%)
未做 PERL	0.559	29.14	10.44	0.640	10.44
PERL on CZ-Si	0.562	31.05	12.37	0.707	12.4

由上述結果可知利用 PERL 技術太陽能轉換效率可以有顯著的提升。我們再繼續氧化鋁薄膜作探討，我們利用常壓式有機金屬物化學氣相沈積法沉積氧化鋁薄膜，我們試著改變不同的沉積時間來探討不同的氧化鋁薄膜沉積厚度對於效率是否改變。

圖三為氧化鋁沉積不同時間的 SEM 圖，沉積時間分別為 10 分鐘、15 分鐘、20 分鐘，厚度分別為 100.6nm、165nm、185nm，其成長速率則分別為 10nm/m、13nm/m、4nm/m，此時我們可以發現隨著沉積的時間增加，其氧化鋁薄膜沉積速率也逐漸下降。



圖三、由上至下分別為沉積氧化鋁薄膜 10 分鐘、15 分鐘、20 分鐘的 SEM 圖

此時我們再將沉積不同時間的氧化鋁薄膜作成太陽能電池元件並用 I-V 量測太陽能轉換效率，表二為量測結果。表二結果顯示，隨著氧化鋁薄膜度增加，太陽能轉換效率會逐漸下降，在此我們可以知道太陽能轉換效率是會被氧化鋁薄膜沉積的厚度所影響。

表二、利用 APMO-CVD 改變氧化鋁的沉積時間，在 AM=1.5 下，I-V 量測太陽能轉換效率。

	Voc (V)	Isc(mA)	Pm(mW)	FF(%)	Eff(%)
Δt =10min	0.56	31.05	12.37	0.70	12.37
Δt =15min	0.56	31.45	11.9	0.67	11.90
Δt =20min	0.56	28.43	11.31	0.70	11.31

4.結論

原子層沉積法（Atomic Layer Deposition, ALD）是現今沉積氧化鋁薄膜較常見的方式，但因為此方法較昂貴且生產量小，所以我們利用常壓式有機金屬物化學氣相沈積法（APMO-CVD）沉積氧化鋁可以有效降低生產成本，在本研究裡氧化鋁薄膜成長最佳條件為 450℃、10 分鐘，再利用 PERL(passivated emitter, rear locally-diffused)技術可以有效提高單晶矽的太陽能轉換效率，此技術有背面鈍化效果，並可以增加少數載子壽命。我們將未經過 PERL 技術處理的太陽能電池元件與有使用 PERL 技術的太陽能電池元件比較，有使用 PERL 技術其太陽能轉換效率可達 12.4%，明顯提升近 2%的效率。

此外，我們發現氧化鋁薄膜沉積時間不同也會改變其太陽能轉換效率，隨著氧化鋁沉積時間增加，太陽能轉換效率也會逐漸下降。

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